AMENDMENTS TO THE CLAIMS

Please cancel claims 1-30 without prejudice.

1-30. (Cancelled)

Please add the following new claims:

31. (New) A processor comprising:

an execution unit, the execution unit to execute instructions; and

a buffer to store data regarding a plurality of instructions executed by the execution unit, wherein the data stored for each executed instruction includes an instruction address and an effective address for the executed instruction;

wherein the storage of data in the buffer is to be halted upon the occurrence of an event, and wherein the processor is to determine a relationship between a set of executed instructions based on the stored data for the set of executed instructions in the buffer.

32. (New) The processor of claim 31, wherein determining a relationship between a set of executed instructions includes determining a base address for each of the set of executed instructions.

33. (New) The processor of claim 31, wherein the buffer comprises a circular buffer.

34. (New) The processor of claim 31, further comprising a filter, the filter determining whether the execution of each of the plurality of memory operations meets a criterion for storage.

35. (New) The processor of claim 34, wherein the filter criterion is based upon

whether the instruction is a stack memory access;

whether an instruction address is within an address range.

whether an effective address is within an address range.

whether data latency is within a latency range

wherein a memory operation is one of a set of memory operation types; or

wherein a memory operation loads or stores a pointer value.

36. (New) The processor of claim 31, wherein the event comprises a miss in a cache, a memory exception, or a programmed event that matches one or more criteria.

37. (New) The processor of claim 36, wherein the criteria include one or more of an invalid effective address or an address that matches a particular range of addresses.

38. (New) The processor of claim 31, wherein the buffer is a part of performance monitoring hardware to monitor processor operations to provide data points regarding the executed loads to software.

39. (New) A method comprising:

monitoring the execution of a plurality of memory operations by a processor;

storing information in a buffer regarding the execution of the plurality of memory operations, the address information including an instruction address and an effective address;

halting the storing of information in the buffer upon the occurrence of an event; and

determining a relationship between a set of memory operations based at least in part on the stored address information for the memory operations.

40. (New) The method of claim 39, wherein the buffer is implemented in hardware.

41. (New) The method of claim 39, wherein determining the relationship includes determining the base address of each memory operation based on the stored information.

42. (New) The method of claim 39, further comprising deleting the oldest information in the buffer when new information regarding the execution of a load is stored.

43. (New) The method of claim 39, further comprising filtering each of the plurality of memory operations to determine whether to store information regarding the execution of the operation in the buffer.

44. (New) The method of claim 39, wherein the event comprises a miss in a cache, a memory exception, or a programmed event that matches one or more criteria.

45. (New) The method of claim 44, wherein the criteria include one or more of an invalid effective address or an address that matches a particular range of addresses.

46. (New) A system comprising:

a bus;

a processor coupled to the bus, the processor comprising:

an execution unit to execute instructions;

performance monitoring hardware to monitor operations of the execution unit, the performance monitoring hardware including a buffer to store data regarding each of a plurality of instructions executed by the processor, data to include an instruction address and an effective address for each executed instruction, the performance monitoring hardware to halt the storing of data in the buffer upon the occurrence of an event and to determine a relationship between a set of instructions based at least in part on the stored data for the instructions; and

a cache memory.

47. (New) The system of claim 46, wherein the buffer comprises a circular buffer.

48. (New) The system of claim 46, further comprising a filter, the filter to determine whether the execution of an instruction meets a criterion for storage.

49. (New) The system of claim 46, wherein the event comprises a miss in the cache memory, a memory exception, or a programmed event that matches a criterion.

50. (New) The method of claim 46, wherein the buffer further includes a base address for each executed instruction.